

**Amendments to the Specification:**

On page 1, line 4, insert the following new section:

**CROSS REFERENCE TO RELATED APPLICATIONS**

This application is a division of U.S. Patent Application Ser. No.10/047,964 filed January 15, 2002.

Amend the paragraph at page 2, line 12 to page 3, line 3 as follows:

Figure 1 illustrates a conventional BEOL interconnect structure utilizing copper metallization and the protective cap layers described above. The interconnect structure comprises a lower substrate 10 which may contain logic circuit elements such as transistors. A dielectric layer 12, commonly known as an inter-level layer dielectric (ILD), overlies the substrate 10. ILD layer 12 may be formed of silicon dioxide (SiO<sub>2</sub>). However, in advanced interconnect structures, ILD layer 12 is preferably a low-k polymeric thermoset material such as SiLK™ (an aromatic hydrocarbon thermosetting polymer available from The Dow Chemical Company). An adhesion promoter layer 11 may be disposed between the substrate 10 and ILD layer 12. A layer of silicon nitride 13 is optionally disposed on ILD layer 12. Silicon nitride layer 13 is commonly known as a hardmask layer or polish stop layer. At least one conductor 15 is embedded in ILD layer 12. Conductor 15 is preferably copper in advanced interconnect structures, but alternatively may be aluminum or other conductive material. When conductor 15 is copper, a diffusion barrier liner 14 is preferably disposed between ILD layer 12 and conductor 15. Diffusion barrier liner 14 is typically comprised of tantalum, titanium, tungsten or nitrides of these metals. The top surface of conductor 15 is made coplanar with the top surface of silicon nitride layer 13, usually by a chemical-mechanical polish

(CMP) step. A cap layer 16, also typically of silicon nitride, is disposed on conductor 15 and silicon nitride layer 13. Cap layer 16 acts as a diffusion barrier to prevent diffusion of copper from conductor 15 into the surrounding dielectric material during subsequent processing steps.

Amend the paragraph at page 3, lines 4-21 as follows:

A first interconnect level is defined by adhesion promoter layer 11, ILD layer 12, silicon nitride layer 13, diffusion barrier liner 14, conductor 15, and cap layer 16 in the interconnect structure shown in Figure 1. A second interconnect level, shown above the first interconnect level in Figure 1, includes adhesion promoter layer 18 47, ILD layer 19 48, silicon nitride layer 20 49, diffusion barrier liner 21 20, conductor 22 24, and cap layer 23 22. The first and second levels may be formed by conventional damascene processes. For example, formation of the second interconnect level begins with deposition of adhesion promoter layer 18 47. Next, the ILD material 19 48 is deposited onto adhesion promoter layer 18 47. If the ILD material is a low-k polymeric thermoset material such as SiLK™, the ILD material is typically spin-applied, given a post apply hot bake to remove solvent, and cured at elevated temperature. Next, silicon nitride layer 20 49 is deposited on the ILD. Silicon nitride layer 20 49, ILD layer 19 48, adhesion promoter layer 18 47 and cap layer 16 are then patterned, using a conventional photolithography and etching process, to form at least one trench and via. The trenches and vias are typically lined with diffusion barrier liner 21 20. The trenches and vias are then filled with a metal such as copper to form conductor 22 24 in a conventional dual damascene process. Excess metal is removed by a CMP process. Finally, cap layer 23 22 is deposited on copper conductor 22 24 and silicon nitride layer 20 49.

Amend the paragraph at page 8, lines 1-11 as follows:

Referring to Figure 2, a preferred embodiment of the interconnect structure of the invention comprises a lower substrate 110 which may contain logic circuit elements such as transistors. A dielectric layer 112, commonly known as an inter-level ~~layer~~ dielectric (ILD), overlies the substrate 110. An adhesion promoter layer 111 may be disposed between the substrate 110 and ILD layer 112. A hardmask layer 113 is preferably disposed on ILD layer 112. At least one conductor 115 is embedded in ILD layer 112 and hardmask layer 113. A diffusion barrier liner 114 may be disposed between ILD layer 112 and conductor 115. The top surface of conductor 115 is made coplanar with the top surface of hardmask layer 113, usually by a chemical-mechanical polish (CMP) step. A first cap layer 116 is disposed on conductor 115 and hardmask layer 113, and a second cap layer 117 is disposed on first cap layer 116.

Amend the paragraph at page 8, lines 12-17 as follows:

A first interconnect level is defined by adhesion promoter layer 111, ILD layer 112, hardmask layer 113, diffusion barrier liner 114, conductor 115, first cap layer 116, and second cap layer 117 in the interconnect structure shown in Figure 2. A second interconnect level, shown above the first interconnect level in Figure 2, includes adhesion promoter layer 118, ILD layer ~~layers~~ 119, hardmask layer 120, diffusion barrier liner 121, conductor 122, first cap layer 123, and second cap layer 124.

Amend the paragraph at page 8, line 18 to page 9, line 11 as follows:

ILD layers 112 and 119 may be formed of any suitable dielectric material, although low-k dielectric materials are preferred. Suitable dielectric materials include carbon-doped silicon dioxide materials; fluorinated silicate glass (FSG); organic polymeric thermoset materials, silicon oxycarbide; SiCOH dielectrics; fluorine doped

silicon oxide; spin-on glasses; silsesquioxanes, including hydrogen silsesquioxane (HSQ), methyl silsesquioxane (MSQ) and mixtures or copolymers of HSQ and MSQ; benzocyclobutene (BCB) -based polymer dielectrics, and any silicon-containing low-k dielectric. Examples of spin-on low-k films with SiCOH-type composition using silsesquioxane chemistry include HOSP™ (available from Honeywell), JSR 5109 and 5108 (available from Japan Synthetic Rubber), Zirkon™ (available from Shipley Microelectronics, a division of Rohm and Haas), and porous low-k (ELk) materials (available from Applied Materials). Examples of carbon-doped silicon dioxide materials, or organosilanes, include Black Diamond™ (available from Applied Materials) and Coral™ (available from Novellus). An example of an HSQ material is FOx™ (available from Dow Corning). For this embodiment, preferred dielectric materials are organic polymeric thermoset materials, consisting essentially of carbon, oxygen and hydrogen. Preferred dielectric materials include the low-k polyarylene ether polymeric material known as SiLK™ (available from The Dow Chemical Company), and the low-k polymeric material known as FLARE™ (available from Honeywell). ILD layers 112 and ~~119~~ 448 may each be about 100 nm to about 1000 nm thick, but these layers are each preferably about 600 nm thick. The dielectric constant for ILD layers 112 and ~~119~~ 448 is preferably about 1.8 to about 3.5, and most preferably about 2.5 to about 2.9.

Amend the paragraph at page 9, lines 12-18 as follows:

Alternatively, ILD layers 112 and ~~119~~ 448 may be formed of a porous dielectric material, such as MesoELK™ (available from Air Products) and XLK™ (a porous version of FOx, available from Dow Corning). For example, If ILD layers 112 and ~~119~~ 448 are formed of such porous dielectric material, the dielectric constant of these layers is preferably less than about 2.6, and is most preferably about 1.5 to 2.5. It is particularly preferred to use an organic polymeric thermoset material having a dielectric constant of about 1.8 to 2.2.

Amend the paragraph at page 10, lines 7-12 as follows:

Conductors 115 and 122 may be formed of any suitable conductive material, such as copper or aluminum. Copper is particularly preferred as the conductive material, due to its relatively low resistance. Copper conductors 115 and 122 ~~121~~ may contain small concentrations of other elements. Diffusion barrier liners 114 and 121 ~~120~~ may comprise one or more of the following materials: tantalum, titanium, tungsten and the nitrides of these metals.

Amend the paragraph at page 15, line 21 to page 16, line 2 as follows:

Following formation of trench 115a, the trench is preferably lined with diffusion barrier liner 114, and then a conductive material is deposited in trench 115a to form conductor 115. Diffusion barrier liner 114 may be deposited by any suitable method, such as by physical vapor deposition (PVD), chemical vapor deposition (CVD) or ionized physical vapor deposition (I-PVD). Conductive material 115 may be deposited in trench 115a by any suitable method, such as by plating technology. Excess liner 114 and conductive material 115 may be removed in a CMP process, in which the top surface of conductor 115 is made coplanar with the top surface of hardmask layer 113. Hardmask layer 113 may serve as a polish-stop layer during this CMP step, thereby protecting ILD layer 112 from damage during polishing. Sacrificial hardmask layers (not shown) may also be removed during this CMP step.

Amend the paragraph at page 20, lines 7-16 as follows:

Following formation of via 122a and trench 122b, the via and trench are preferably lined with diffusion barrier liner 121, and then a conductive material is

deposited in the via and trench to form conductor 122, as shown in Figure 3(i). Diffusion barrier liner 121 may be deposited by the same method used for diffusion barrier liner 114, and conductive material 122 may be deposited by the same method used for conductor 115. Excess liner 121 ~~120~~ and conductive material 122 ~~121~~ may be removed in a CMP process, in which the top surface of conductor 122 ~~121~~ is made coplanar with the top surface of hardmask layer 120 ~~119~~. Sacrificial hardmask layers (not shown) may also be removed during this CMP step. Hardmask layer 120 ~~119~~ may serve as a polish-stop layer during this CMP step, thereby protecting ILD layer 119 ~~118~~ from damage during polishing.